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EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,652	THOMPSON, KERRY	
	Examiner	Art Unit	
	Joni Hsu	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5, 8-12* is/are rejected.

7)☒ Claim(s) *6,7 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-3, 8, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams (US 20040207618A1) in view of Simmonds (US006646645B2), further in view of Srivastava (US005121086A).

4. With regard to Claim 1, Williams describes an external synchronization signal (207, Figure 2D) [0061] or video synchronization signal, which is inherently sent from a remote computer since it is an external signal. Therefore, Williams describes a method for filtering a

video synchronization signal sent from a remote computer to a master graphics processing computer (203-1) [0087]. The video synchronization signal is then sent from the master graphics processing computer to a plurality of graphics processing computers (203-N) [0088]. Therefore, the video synchronization signal is sent from the remote computer to a plurality of graphics processing computers, each graphics processing computer having at least one graphics processing card (208) and a sync filter (213) [0087-0088]. The external synchronization signal has a phase [0087], and this phase inherently refers to the spacing of the sync signals in the external synchronization signal. Therefore, Williams describes receiving a stream of at least n sync signals from the remote computer. The controller in the master graphics module compares the phase of the clock signal with the phase of the external synchronization signal. If the phase of the clock signal is not in synchronization with the phase of the external synchronization signal, then the frequency of the clock generator is adjusted to match the frequency of the external synchronization signal [0087]. Then the slave graphics modules compare the phase of the timing signal from the master graphics module with its own timing signal. If the phase of the timing signal from the master graphics module is not in synchronization with the phase of its own timing signal, then the frequency of the clock generator of the slave graphics modules are adjusted to the frequency of the timing signal of the master graphics module [0088]. The clock signals of the graphics modules are the n sync signals since they are inherently the signals that were received previously, and the external synchronization signal is the n + 1 sync signal since it is the signal that is received next. Therefore, Williams describes comparing an n + 1 sync signal with each of the n sync signals to form a comparison for each of the n sync signals. The n sync signals are being replaced with the n + 1 sync signal, and therefore an oldest of the n sync signals

is being replaced with the n + 1 sync signal. The n + 1 sync signal is used to synchronize the at least one graphics processing card in each graphics processing computer with each at least one graphics processing card in the plurality of graphics processing computers if the n sync signals are not in synchronization with the n + 1 sync signal [0087-0088].

However, Williams does not specifically teach that the most recently received n sync signals are stored in an array. However, Simmonds describes that a sync card (100A, Figure 3) on a remote computer (50A; Col. 6, lines 56-57) acts as a master sync card for the reference clock while all other sync cards, e.g., sync cards 100B, 100C, serve as slaves and use the reference clock of the master sync card 100A. The reference clock generated by the master sync card 100A is distributed and utilized by all sync cards 100A-C (Col. 7, lines 16-22). Therefore, Simmonds describes a method for filtering a video synchronization signal (reference clock) sent from a remote computer (50A, Figure 3) to a plurality of graphics processing computers (50B, 50C; Col. 7, lines 16-22), each graphics processing computer having at least one graphics processing card (60) and a sync filter (100) (Col. 6, lines 56-62), comprising the steps of receiving a stream of at least n sync signals from the remote computer (reference clock and raster sync signals; Col. 7, lines 16-28). When the sync card feeds multiple PC graphics subsystems, the corresponding multiple graphics processors are generally synchronized to be outputting the same scanline and nearly the same pixel such that signals from only one of the graphics processor is used (Col. 10, lines 12-17). The selected scanline locations are preferably programmed into the registers (146, 148, Figure 6; Col. 10, lines 26-28). Figure 7 shows an alternative scheme which is similar to the scheme in Figure 6, except that a clock counter is used instead of a scanline counter and the values loaded into the registers (246, 248) are in units of

clocks rather than scanlines (Col. 10, lines 30-41). Therefore, the values stored in the registers or array are the most recently received n sync signals. The signals are then compared (Col. 10, lines 37-46).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Willaims so that the most recently received n sync signals are stored in an array as suggested by Simmonds because Simmonds suggests that the signals need to be stored first in order to be compared (Col. 10, lines 37-46). This is well-known in the art.

However, Williams and Simmonds do not teach synchronizing if the comparisons of the n sync signals are greater on the average than a preset threshold. However, Srivastava describes synchronizing display scan systems (Col. 1, lines 6-8). The threshold detector (60, Figure 3) responds to detect large frequency corrections (Col. 6, lines 1-4). If the frequency error is substantial, the output of the error amplifier applied to the threshold detector exceeds the upper threshold therein producing an output signal at terminal 61 (Col. 8, lines 19-22). The output signal at terminal 61 is coupled to the error integrator (Col. 8, lines 22-25, 48-50). This error integrator averages the output. If the average error is many times down, then the up/down counter is clocked down. The process repeats till the error is reduced and the limit decoder stops providing the excitation at the up/down counter's input terminal (Col. 8, lines 50-61), therefore synchronizing the signal. Therefore, Srivastava describes synchronizing if the comparisons of the n sync signals are greater on the average than a preset threshold.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Willaims and Simmonds to include synchronizing if the comparisons of the n sync signals are greater on the average than a preset threshold as suggested

by Srivastava. Srivastava suggests that if a conventional phase locked loop is used and a substantial frequency difference exists between the frequency of signals and the reference synchronizing signals, there will be a large static phase error (Col. 3, lines 44-66). By averaging the n sync signals and having a threshold, the short duration or small magnitude frequency and phase correction are ignored and instead the system responds solely to large magnitude frequency corrections having an extended duration. The system responds to these average changes to apply a steady state signal which, in effect, removes the need for the large magnitude long duration corrections and avoids objectionable static phase error (Col. 5, line 61-Col. 6, line 10; Col. 8, lines 61-65).

5. With regard to Claim 2, Williams describes each of the graphics modules (103, Figure 1B) are in separate remote computers (10) [0050]. Therefore, the step of receiving an array of n sync signals includes the more specific step of receiving the array of n sync signals at one or more remote computers.

6. With regard to Claim 3, Williams describes that the one or more remote computers (10, Figure 1B) are used to generate graphical images (controlling image content provided to multiple projectors (102)) [0048, 0050].

7. With regard to Claim 8, Williams describes the step of operating the sync filter (213, Figure 2D) in the plurality of graphics processing computers (203) [0087-0088].

8. With regard to Claim 10, Williams describes an external synchronization signal (207, Figure 2D) [0061] or video synchronization signal, which is inherently sent from a remote computer since it is an external signal. Therefore, Williams describes a system for filtering a video synchronization signal from a remote computer with a sync filter (213-1), to a master graphics processing computer (203-1) [0087]. The video synchronization signal is then sent from the master graphics processing computer to a plurality of graphics processing computers (203-N) [0088]. Therefore, there is a dedicated network for sending sync signals from the remote computer to a plurality of graphics processing computers, each graphics processing computer in communication with a sync filter (213) [0087-0088]. The sync filter (213-1) in the master graphics module compares the phase of the clock signal with the phase of the external synchronization signal. If the phase of the clock signal is not in synchronization with the phase of the external synchronization signal, then the frequency of the clock generator is adjusted to match the frequency of the external synchronization signal [0087]. Then the sync filters (213-N) in the slave graphics modules compare the phase of the timing signal from the master graphics module with its own timing signal. If the phase of the timing signal from the master graphics module is not in synchronization with the phase of its own timing signal, then the frequency of the clock generator of the slave graphics modules are adjusted to the frequency of the timing signal of the master graphics module [0088]. The clock signals of the graphics modules are the n sync signals since they are inherently the signals that were received previously, and the external synchronization signal is the n + 1 sync signal since it is the signal that is received next. Therefore, Williams describes that the sync filter has a processor configured to compare an n + 1 sync signal with each of the n sync signals to form a comparison for each of the n sync signals.

The n sync signals are being replaced with the n + 1 sync signal, and therefore the processor is further configured to replace an oldest of the n sync signals with the n + 1 sync signal. The processor is further configured to send the n + 1 sync signal to synchronize the plurality of graphics processing computers if the n sync signals are not in synchronization with the n + 1 sync signal [0087-0088].

However, Williams does not specifically teach that the sync filter has a memory device configured to store an array of n sync signals. However, Simmonds describes that a sync card (100A, Figure 3) on a remote computer (50A; Col. 6, lines 56-57) acts as a master sync card for the reference clock while all other sync cards, e.g., sync cards 100B, 100C, serve as slaves and use the reference clock of the master sync card 100A. The reference clock generated by the master sync card 100A is distributed and utilized by all sync cards 100A-C (Col. 7, lines 16-22). Therefore, Simmonds describes a method for filtering a video synchronization signal (reference clock) sent from a remote computer (50A, Figure 3) to a plurality of graphics processing computers (50B, 50C; Col. 7, lines 16-22), each graphics processing computer having at least one graphics processing card (60) and a sync filter (100) (Col. 6, lines 56-62), comprising the steps of receiving a stream of at least n sync signals from the remote computer (reference clock and raster sync signals; Col. 7, lines 16-28). When the sync card feeds multiple PC graphics subsystems, the corresponding multiple graphics processors are generally synchronized to be outputting the same scanline and nearly the same pixel such that signals from only one of the graphics processor is used (Col. 10, lines 12-17). The selected scanline locations are preferably programmed into the registers (146, 148, Figure 6; Col. 10, lines 26-28). Figure 7 shows an alternative scheme which is similar to the scheme in Figure 6, except that a clock counter is used

instead of a scanline counter and the values loaded into the registers (246, 248) are in units of clocks rather than scanlines (Col. 10, lines 30-41). Therefore, the values stored in the registers are the n sync signals, and the sync filter (200) has a memory device (246, 248) configured to store an array of n sync signals. The signals are then compared (Col. 10, lines 37-46). This would be obvious for the same reasons given in the rejection for Claim 1.

However, Williams and Simmonds do not teach synchronizing if the comparisons are averagely greater than a preset threshold. However, Srivastava describes synchronizing display scan systems (Col. 1, lines 6-8). The threshold detector (60, Figure 3) responds to detect large frequency corrections (Col. 6, lines 1-4). If the frequency error is substantial, the output of the error amplifier applied to the threshold detector exceeds the upper threshold therein producing an output signal at terminal 61 (Col. 8, lines 19-22). The output signal at terminal 61 is coupled to the error integrator (Col. 8, lines 22-25, 48-50). This error integrator averages the output. If the average error is many times down, then the up/down counter is clocked down. The process repeats till the error is reduced and the limit decoder stops providing the excitation at the up/down counter's input terminal (Col. 8, lines 50-61), therefore synchronizing the signal. Therefore, Srivastava describes synchronizing if the comparisons are averagely greater than a preset threshold. This would be obvious for the same reasons given in the rejection for Claim 1.

9. Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams (US 20040207618A1) in view of Simmonds (US006646645B2), further in view of Srivastava (US005121086A), further in view of Cheung (US006538656B1).

10. With regard to Claim 4, Williams, Simmonds, and Srivastava are relied upon for the teachings as discussed above relative to Claim 1. Williams describes the step of comparing an n + 1 sync signal with each of the n sync signals, as discussed in the rejection for Claim 1.

However, Williams does not teach averaging the n sync signals in the array and using the n + 1 sync signal if the average of the n sync signals in the array is greater than a preset threshold. However, Srivastava describes synchronizing display scan systems to the reference synchronizing signals (Col. 1, lines 6-8; Col. 2, lines 20-43). The threshold detector (60, Figure 3) responds to detect large frequency corrections (Col. 6, lines 1-4). If the frequency error is substantial, the output of the error amplifier applied to the threshold detector exceeds the upper threshold therein producing an output signal at terminal 61 (Col. 8, lines 19-22). The output signal at terminal 61 is coupled to the error integrator (Col. 8, lines 22-25, 48-50). This error integrator averages the output. If the average error is many times down, then the up/down counter is clocked down. The process repeats till the error is reduced and the limit decoder stops providing the excitation at the up/down counter's input terminal (Col. 8, lines 50-61), therefore synchronizing the signals to the reference synchronizing signals. The reference synchronizing signals are considered to be the n + 1 sync signals and the signals that are synchronized to it are considered to be the n sync signals. Therefore, Srivastava describes averaging the n sync signals in the array and using the n + 1 sync signal if the average of the n sync signals in the array is greater than a preset threshold. This would be obvious for the same reasons given in the rejection for Claim 1.

However, Williams and Srivastava do not teach computing a vote for each of the comparisons of the n sync signals in the array. However, Cheung describes a video and graphics

system with a data transport processor (Col. 2, lines 23-39). The measurement of the horizontal line time is done at a sub-sample accuracy (Col. 38, lines 20-22). The horizontal sync tracker uses a sub-sample interpolation technique to obtain an accurate measurement of sync edge location. Three values are used to determine the sub-sample accuracy. The three values are the threshold level (T), the value of the sample that crossed the threshold level (V2) and the value of the previous sample that did not cross the threshold level (V1). The sub-sample value is the ratio of (T-V1)/(V2-V1) (Col. 38, line 57-Col. 39, line 7). Therefore the sub-sample value is a vote, and a vote is computed for each of the comparisons of the n sync signals in the array.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Williams and Srivastava to include computing a vote for each of the comparisons of the n sync signals in the array as suggested by Cheung because Cheung suggests that by computing a vote, the accuracy of the signal can be determined and the signal can be modified to obtain the most accurate signal (Col. 38, line 63-Col. 39, line 7).

11. With regard to Claim 11, Williams describes that the processor is configured to compare an n + 1 sync signal with each of the n sync signals and send the n + 1 sync signals to synchronize the plurality of graphics processing computers if the n sync signals are not in synchronization with the n + 1 sync signal, as discussed in the rejection for Claim 1.

However, Williams does not teach that the processor is configured to average the n sync signals in the array and send the n + 1 sync signals for synchronization if the average of the n sync signals in the array is computed to be greater than a preset threshold. However, Srivastava describes synchronizing display scan systems to the reference synchronizing signals (Col. 1,

lines 6-8; Col. 2, lines 20-43). The threshold detector (60, Figure 3) responds to detect large frequency corrections (Col. 6, lines 1-4). If the frequency error is substantial, the output of the error amplifier applied to the threshold detector exceeds the upper threshold therein producing an output signal at terminal 61 (Col. 8, lines 19-22). The output signal at terminal 61 is coupled to the error integrator (Col. 8, lines 22-25, 48-50). This error integrator averages the output. If the average error is many times down, then the up/down counter is clocked down. The process repeats till the error is reduced and the limit decoder stops providing the excitation at the up/down counter's input terminal (Col. 8, lines 50-61), therefore synchronizing the signals to the reference synchronizing signals. The reference synchronizing signals are considered to be the n + 1 sync signals and the signals that are synchronized to it are considered to be the n sync signals. Therefore, Srivastava describes that the processor is configured to average the n sync signals in the array and send the n + 1 sync signals for synchronization if the average of the n sync signals in the array is greater than a preset threshold. This would be obvious for the same reasons given in the rejection for Claim 1.

However, Williams and Srivastava do not teach that the processor is further configured to compute a vote for each of the comparisons of the n sync signals in the array. However, Cheung describes a video and graphics system with a data transport processor (Col. 2, lines 23-39). The measurement of the horizontal line time is done at a sub-sample accuracy (Col. 38, lines 20-22). The horizontal sync tracker uses a sub-sample interpolation technique to obtain an accurate measurement of sync edge location. Three values are used to determine the sub-sample accuracy. The three values are the threshold level (T), the value of the sample that crossed the threshold level (V2) and the value of the previous sample that did not cross the threshold level

(V1). The sub-sample value is the ratio of (T-V1)/(V2-V1) (Col. 38, line 57-Col. 39, line 7). Therefore the sub-sample value is a vote, and the processor is configured to compute a vote for each of the comparisons of the n sync signals in the array. This would be obvious for the same reasons given in the rejection for Claim 4.

12. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams (US 20040207618A1) in view of Simmonds (US006646645B2), further in view of Srivastava (US005121086A), further in view of Cheung (US006538656B1), further in view of Miner (US006690655B1).

13. With regard to Claim 5, Williams, Simmonds, Srivastava, and Cheung are relied upon for the teachings as discussed above relative to Claim 4. Williams describes initializing a filter (213, Figure 2D) with the n sync signals [0087].

However, Williams, Simmonds, Srivastava, and Cheung do not teach a method of synchronizing using an array of n time stamps of the n sync signals. However, Miner describes a network with multiple remote interface units (RIU, 209, 210, Figure 2; Col. 4, lines 49-53). The RIUs are synchronized by receiving an array of n time stamps of the n sync signals (Col. 13, lines 14-28; Col. 15, lines 32-39).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Williams, Simmonds, Srivastava, and Cheung to include a method of synchronizing using an array of n time stamps of the n sync signals as suggested by Miner because Miner suggests that by using time stamps, the system can determine when each

sync signal is received (Col. 13, lines 14-28). By doing so, the system can detect if a RIU has not received a sync signal within a threshold period of time, and if so, the RIU is re-synchronized (Col. 15, lines 32-39). If a RIU has not received a sync signal within a threshold period of time, it results in the loss of synchronization (Col. 13, lines 4-10). Therefore, by using time stamps, the system can assure that the RIUs stay synchronized.

14. With regard to Claim 12, Simmonds describes that the memory is configured to store an array of the n sync signals, as discussed in the rejection for Claim 10.

However, Simmonds does not teach a method of synchronizing using an array of n time stamps of the n sync signals. However, Miner describes a network with multiple remote interface units (RIU, 209, 210, Figure 2; Col. 4, lines 49-53). The RIUs are synchronized by receiving an array of n time stamps of the n sync signals (Col. 13, lines 14-28; Col. 15, lines 32-39). This would be obvious for the same reasons given in the rejection for Claim 5.

15. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Williams (US 20040207618A1) in view of Simmonds (US006646645B2), further in view of Srivastava (US005121086A), further in view of Kennedy (US 20050093854A1).

Williams, Simmonds, and Srivastava are relied upon for the teachings as discussed above relative to Claim 8.

However, Williams, Simmonds, and Srivastava do not teach the step of operating the sync filter as software in the plurality of graphics processing computers. However, Kennedy

describes the step of operating the sync filter (106, Figure 3) [0033] as software [0035] in the plurality of graphics processing computers (102, Figure 1) [0029].

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Williams, Simmonds, and Srivastava to include the step of operating the sync filter as software in the plurality of graphics processing computers as suggested by Kennedy because Kennedy suggests that synchronizations is made more difficult by the varying complexities of the images being presented on the various displays. As a result, many graphics systems will become desynchronized and/or produce visual artifacts or distortions in the resulting image [0009]. Therefore, operating the sync filter as software has the advantage of being able to program the phase-locked loop so that its speed can be adjusted to react more quickly or more slowly to changes [0017].

Allowable Subject Matter

16. Claims 6, 7, and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. The following is a statement of reasons for the indication of allowable subject matter:

The prior art taken singly or in combination do not teach or suggest finding a comparison time that is an absolute time nearest to the n time stamp by subtracting an integer multiple of a base time period until the comparison time is within plus or minus one half of the base time period; comparing an absolute value of the comparison time with a known-bad threshold wherein

a vote of zero occurs if the difference exceeds the known-bad threshold; and computing the vote as a linear interpolation between zero and the known-bad threshold as recited in Claims 6 and 13. The prior art also does not teach computing the vote as a linear interpolation equal to one minus the ratio of the absolute value of the comparison time that is less than the known-bad threshold and the known-bad threshold as recited in Claims 7 and 13.

18. The closest prior art (Cheung) describes a video and graphics system with a data transport processor (Col. 2, lines 23-39). The measurement of the horizontal line time is done at a sub-sample accuracy (Col. 38, lines 20-22). The horizontal sync tracker uses a sub-sample interpolation technique to obtain an accurate measurement of sync edge location by drawing a straight line between the two successive samples of the horizontal sync signal just above and just below the presumed threshold value to determine where the threshold value has been crossed. Three values are used to determine the sub-sample accuracy. The three values are the threshold level (T), the value of the sample that crossed the threshold level (V2) and the value of the previous sample that did not cross the threshold level (V1). The sub-sample value is the ratio of (T-V1)/(V2-V1). The difference (V2-V1) is divided by 16 to make a variable called DELTA. V1 is then incremented by DELTA until it exceeds the threshold T (Col. 38, line 57-Col. 39, line 7). Therefore the sub-sample value is a vote. However, Cheung does not teach finding a comparison time that is an absolute time nearest to the n time stamp by subtracting an integer multiple of a base time period until the comparison time is within plus or minus one half of the base time period; comparing an absolute value of the comparison time with a known-bad threshold wherein a vote of zero occurs if the difference exceeds the known-bad threshold; and

computing the vote as a linear interpolation between zero and the known-bad threshold and computing the vote as a linear interpolation equal to one minus the ratio of the absolute value of the comparison time that is less than the known-bad threshold and the known-bad threshold.

Prior Art of Record

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US006831648B2 teaches a graphics system and method for performing synchronized image display and swap buffering in a multiple display/multiple processor environment (Col. 1, line 66-Col. 2, line 3).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

Kee M. Tung
Primary Examiner